Today’s Reality

- 38% cite system architecture design and specification as the highest cause of schedule delays

- Quickly followed by system integration, test and software development (all above 25%)

- In 2007 the cost of software development for an SoC surpassed the cost of IC design

Source: VDC and Gary Smith EDA 2007
CoWare SystemC Tools and IP

- CoWare Platform Architect
- CoWare Model Library
- SystemC TLM & SCML
- SystemC Platform Capture and Analysis
- Software Development
- CoWare Virtual Platform
- Optimizing Performance of DSP Algorithms and Programmable IP
- CoWare Model Designer
- Legacy RTL IP Reuse
- CoWare Processor Designer
- CoWare Signal Processing Designer

CoWare SystemC Tools and IP
Modeling TLM Peripherals

- TLM design-task is determined by the bus model
- Separation of behavior, communication and timing
- Re-use peripheral models for multiple design tasks
- Simple modeling pattern
- Supported by standards based SystemC Modeling Library (SCML)
# CoWare IP Model Library

## Processors

<table>
<thead>
<tr>
<th>Cycle Accurate</th>
<th>ARM7, ARM9, ARM11, Cortex R4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tensilica Xtensa</td>
<td>MIPS4KE, MIPS24K, MIPS34K</td>
</tr>
<tr>
<td>IBM PowerPC440</td>
<td>IBM PowerPC750GX</td>
</tr>
<tr>
<td>Toshiba MeP</td>
<td><strong>Ultra-Fast IA</strong></td>
</tr>
<tr>
<td>ARM</td>
<td>ARM7TDMI, ARM926, ARM946, ARM968, ARM1136, ARM1176. ARM11 MPCore Toshiba MeP</td>
</tr>
<tr>
<td>ARM</td>
<td><strong>Fast IA</strong></td>
</tr>
<tr>
<td>Tensilica Xtensa</td>
<td>Tensilica Diamond</td>
</tr>
<tr>
<td>IBM PowerPC440</td>
<td>IBM PowerPC750GX</td>
</tr>
</tbody>
</table>

## Peripherals

<table>
<thead>
<tr>
<th>ARM</th>
<th>SCML PrimeCells in source code: customer can add timing annotation</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>UART (PL011), SSP (PL022), RTC (PL031), GPIO (PL061), DMAC (PL080), SSMC (PL093), GIR (PL140), VIC (PL190), IPCM (PL320), Timer (SP804), Watchdog (SP805), Smart Card Interface (PL130), Color LCD Controller (PL111), Vectored Interrupt Controller (PL192) Multiport Memory Controller (PL171), Multiport Memory Controller (PL175), AXI dynamic memory controller (PL340), AXI static memory controller (PL350)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MeP</th>
<th>SCML GIPL in source code: customer can add timing annotation</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Reset Generator, Clock Generator, Dual-port DMAC, Single-port Memory Controller, Memory, Input Device, Output Device, Interrupt Controller, Timer, Pin Stub, Pin Drive</td>
</tr>
</tbody>
</table>

## Interconnect

<table>
<thead>
<tr>
<th>ARM</th>
<th>AMBA 2.0 Bus Library (BL)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>AMBA3 AXI BL</td>
</tr>
<tr>
<td></td>
<td>Sonics SMX BL</td>
</tr>
<tr>
<td>IBM</td>
<td>IBM CoreConnect BL</td>
</tr>
<tr>
<td>AVF</td>
<td>Simple OCP BL</td>
</tr>
</tbody>
</table>

## Memory Subsystem

<table>
<thead>
<tr>
<th>Sonics</th>
<th>MemMax</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sonics</td>
<td>MemDDR</td>
</tr>
<tr>
<td>PL172 (AHB)</td>
<td></td>
</tr>
<tr>
<td>PL175 (AHB)</td>
<td></td>
</tr>
<tr>
<td>PL340 (AXI)</td>
<td></td>
</tr>
<tr>
<td>PL350 (AXI)</td>
<td></td>
</tr>
<tr>
<td>GMEMSUBSYS</td>
<td></td>
</tr>
<tr>
<td>Denali Memory Models</td>
<td></td>
</tr>
<tr>
<td>by interface to MMAV</td>
<td></td>
</tr>
</tbody>
</table>

- Need standards to maintain and grow IP lib
- IP integration effort is greatly reduced ...
  ... but not completely eliminated
What Does TLM 2.0 Enable for CoWare?

- TLM 2.0 enables re-use of models for multiple design tasks
  - Loosely Timed models can interoperate and can be refined to Approximately Timed
  - LT and AT models can be connected to Cycle Accurate models through transactors

- TLM 2.0 enables high simulation speed for SystemC based Virtual Platforms
  - Simulation speed APIs in CoWare VP are part of TLM 2.0
    - Temporal decoupling, Direct Memory Interface, synchronization on demand

- Interoperability motivates IP vendors to provide standard compliant models

CoWare Value Propositions Are Fully Supported by TLM 2.0
CoWare Support for TLM 2.0

**Initial Release Plan for 2008**
- TLM2 transactor adapters
  - Connect TLM 2.0 models to CoWare buses
  - Connect SCML models to TLM 2.0 buses
  - Full support for DMI “speed interoperability”
- TLM2 bus library
  - LT bus (similar to PV-BL)
  - AT bus (similar to simple_OCP_BL)
- Platform assembly support
  - Import TLM 2.0 models
  - TLM 2.0 protocol libraries
  - TLM 2.0 Easy Connect
- SystemC explorer support
  - TLM 2.0 analysis ports
- SystemC wizard support
  - TLM 2.0 interface generation

**Followed by**
- TLM 2.0 based IP
  - PSPs with native TLM2.0 interfaces
  - Direct transactors from TLM 2.0 to CoWare buses (OCP-IP AHB, AXI, etc.)
- SCML2
  - Native TLM 2.0 infrastructure for SCML, including openly available source code kits

**Assumptions:**
TLM 2.0 ratified by DAC
No major changes to TLM2-D2
Summary

- CoWare solutions are standards-based
  - TLM 2.0 standards are coming in 2008
  - CoWare value propositions are fully supported by TLM 2.0

- CoWare will support both existing and new standards
  - No migration is required
  - Existing customer designs will continue to work fine

- CoWare customers can adopt TLM 2.0 at their own pace
  - We can help with education
  - CoWare’s roadmap will help make for smooth adoption