TLM WG Update

NASCUG VII at DAC

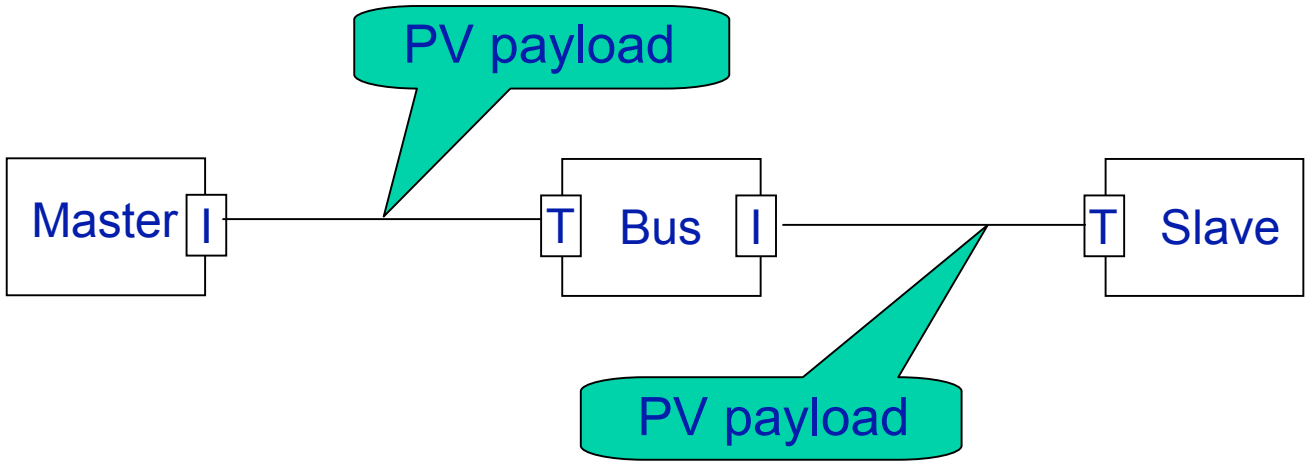
Trevor Wieman, TLM WG Chairman

June 4, 2007

Untimed TLM Modeling

TLM 2.0 Draft #1

- Based on transport core TLM interface
- Uses Programmer's View (PV) payload
- All models using the PV payload and transport core interface can be connected and simulated together



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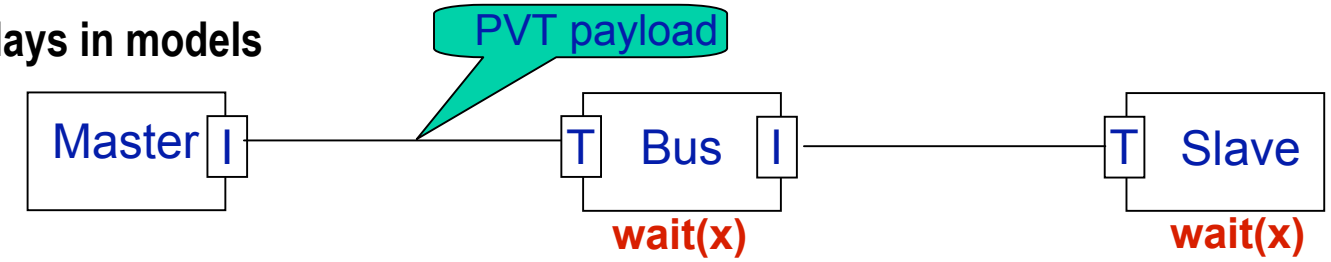
Timed TLM Modeling

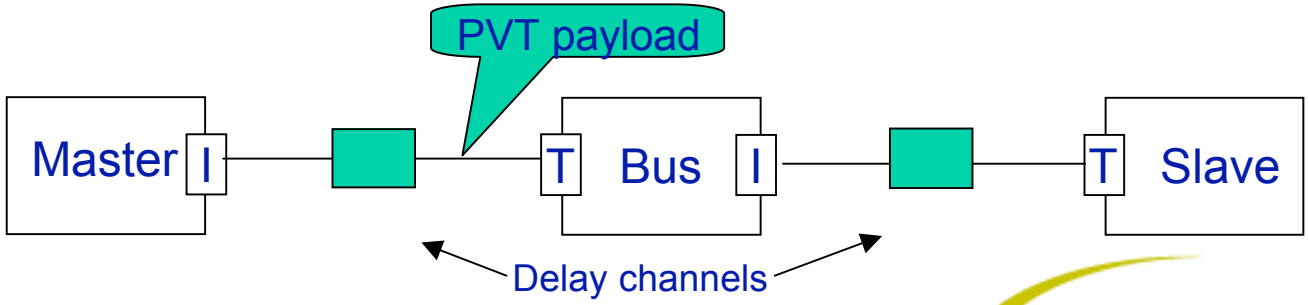
TLM 2.0 Draft #1

- Enable timing annotations of event-based simulations
- Uses PV with Timing (PVT) payload, based on put/get core TLM interfaces
- All models using the PVT payload and put/get core interfaces can be connected and simulated together

- 2 structural approaches supported:
  - 1) Insert delays in models



  - 2) Rely on a "delay channel" between components to take timing delays into account



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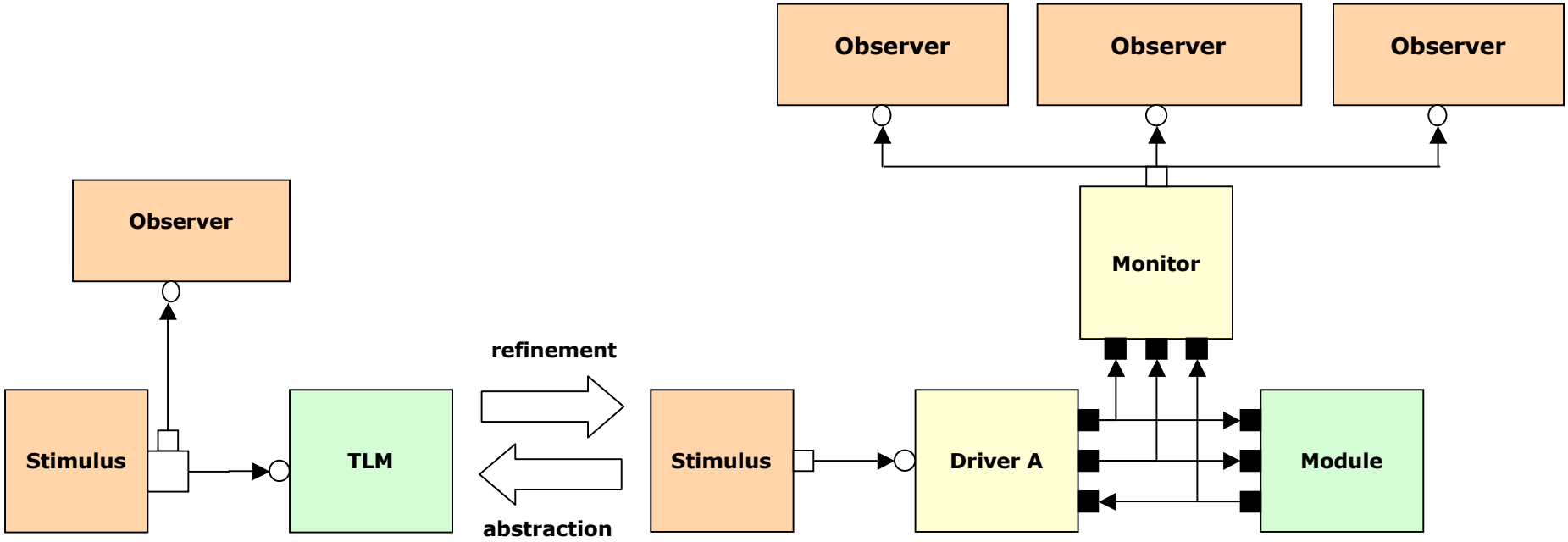
Analysis Ports

TLM 2.0 Draft #1

- Non-intrusive monitoring of transactions going through TLM ports
  - A SystemC implementation of the observer pattern
- Can connect zero, one or many observers to a single analysis port
- Non-blocking, non-negotiated interface



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Key Feedback on the TLM 2.0 Draft #1

- Understanding the Kit and the Methodology
  - More comprehensive documentation and examples should be provided – even for draft releases
  - Relevant abstraction levels should be well defined and documented
  - The requirements specification should be provided
  - The solution's design and the rationale driving it should be better documented

- TLM Interoperability and API specifications
  - DATA_MODE doesn't sufficiently address pass-by-value overhead
  - The payload extension mechanism seems inefficient and overly complex
  - Combining the request and response payloads into a single transaction payload might improve efficiency and simplicity
  - The request and response attributes are non-intuitive and somewhat cumbersome to use
  - A common interface for PV and PVT should be pursued
  - Interoperability with TLM 1.0 must be demonstrated and well documented

Requirements Specification

- Incorporates draft kit feedback, perspective from new participants and insights from new contributions
- Now available from www.systemc.org
  - Review and provide feedback to tlm-2-0-review@systemc.org
- Accompanying whitepaper provides a high-level introduction
- Establishes baseline terminology and identifies target use cases
- Encompasses “untimed” and “approximate-timed” TLM interoperability with a focus on memory-mapped busses

Key TLM Terminology

- The TLM standard will provide interoperability for various "modeling styles"

- Untimed modelling style
  - There is no explicit mention of time or cycles, but addresses concurrency and sequencing of operations.
  - In the absence of any explicit notion of time the sequencing of operations across multiple concurrent threads is accomplished using synchronization primitives such as events, mutexes and blocking FIFOs.

Key TLM Terminology

- **Approximately timed modelling style**
  - There exists a one-to-one mapping between the externally observable states of the model and the states of some corresponding detailed reference model such that the mapping preserves the sequence of state transitions but not their precise timing.
  - The degree of timing accuracy is undefined.

- **Cycle accurate modelling style**
  - Possible to predict the state of the model in any given cycle at the external boundary of the model and thus to establish a one-to-one correspondence between the states of the model and the externally observable states of a corresponding RTL model in each cycle, but which is not required to explicitly re-evaluate the state of the entire model in every cycle or to explicitly represent the state of every boundary pin or internal register.
  - Only applicable to models that have a notion of cycles.

Additional Features

- Untimed modeling
  - Temporal decoupling (untimed master slack scheduling)
  - Untimed model synchronization
  - Direct memory interface
- Instrumentation
  - SCV extensions for transaction data structures
  - Integration of analysis ports with TLM ports
- Miscellaneous
  - Convenience ports with event finder

TLM 2.0 Plans

- TLM 2.0 draft #2
  - Contents:
    - Untimed TLM interoperability ("PV")
    - Preliminary approximate-timed TLM interoperability ("PVT" or "AV")
      - Sufficiently developed to ensure no rework of the untimed TLM
    - Analysis ports
    - Examples and documentation
  - Schedule: release for public review October 31, 2007
    - OSCI has approved funding for contract development assistance
- TLM 2.0 approval
  - Scheduled for December/January
    - Includes feedback from public review plus additional examples and documentation

Thank You

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