High Level Synthesis

Re-usable model of AMBA AXI4 communication protocol for HLS based design flow developed using SystemC Synthesis subset

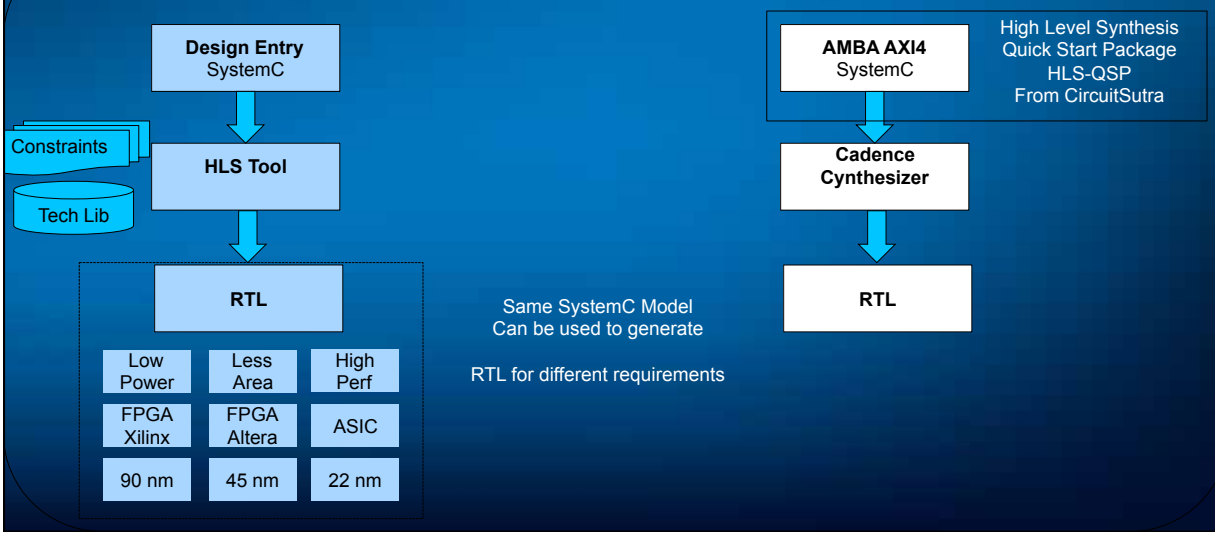
NASCUG, San Francisco, USA (June, 2014)

Presenter
Dinesh Malhotra, CircuitSutra

AUTHORS
Amaranatha reddy, PVS Phaneendra, Umesh Sisodia (CircuitSutra)

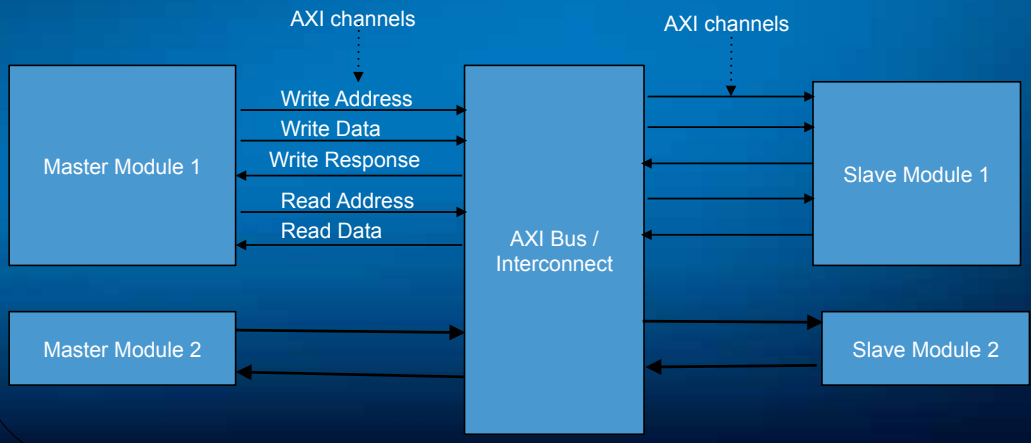
High Level Synthesis - Overview

Raising the abstraction of chip design above RTL

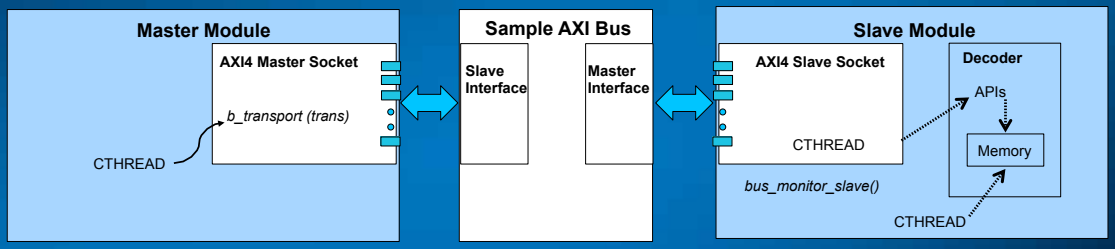


AXI4 Overview

AXI4 (Advanced eXtensible Interface) is latest of AMBA(Advanced Microcontroller Bus Architecture) bus protocols that is useful for on-chip bus designs in SoCs



HLS-QSP for AXI



Reusable Sockets

- AXI Master Socket
- AXI Slave Socket
- Configurable for address width, data width
- Configurable for abstraction: PIN / TLM
- Can be used to design AXI compliant IP

Sample AXI bus

- For demo and testing of sockets

Socket instantiation & binding

In Master Module :

```
axi_master_socket<...>  axi_master_port;
```

In Slave Module :

```
axi_slave_socket<...>  axi_slave_port;
```

Add both sockets to Axi bus :

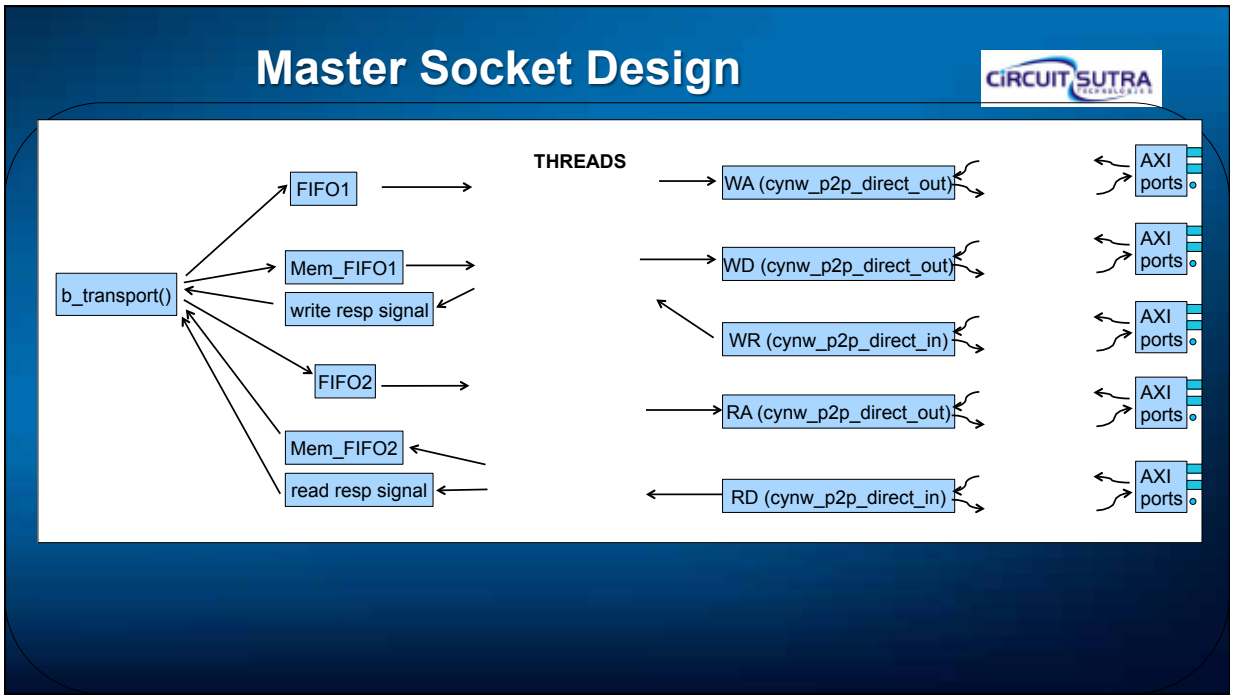
```
axi_bus->add_master(Master_module->axi_master_port);
axi_bus->add_slave(Slave_module->axi_slave_port);
```

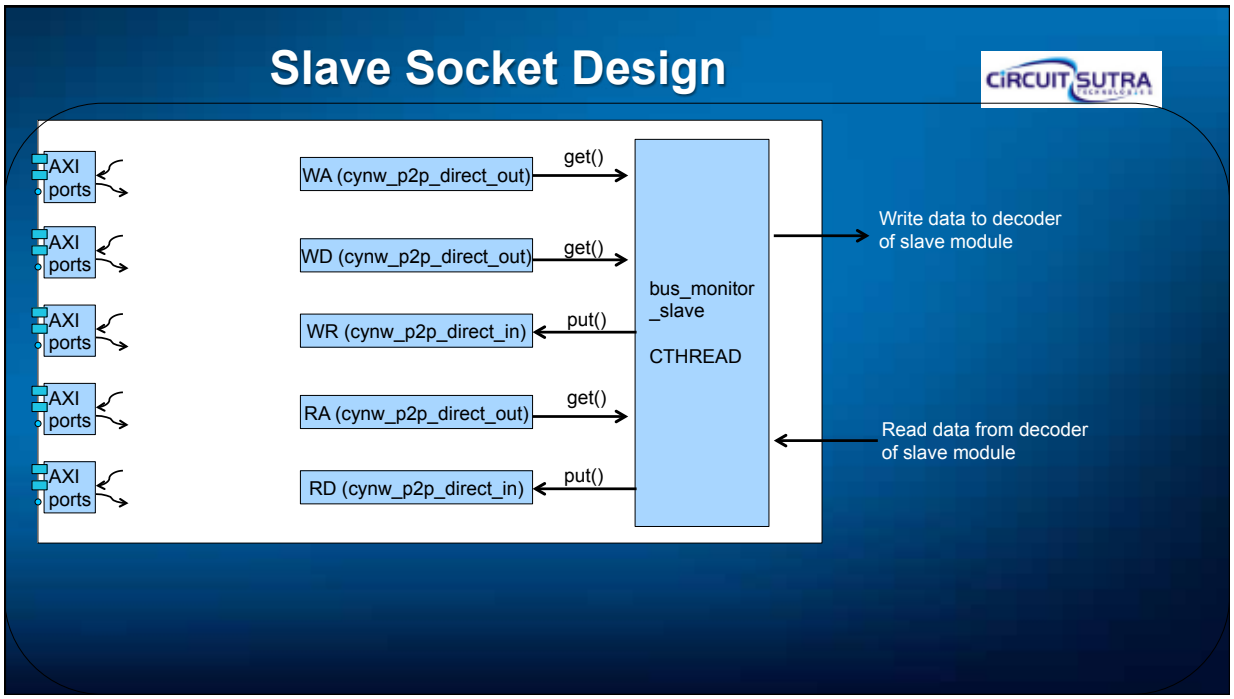
Initiating AXI transaction in Master

```
AXI::AXI_payload trans;

trans.set_streaming_width(1);
trans.set_command(AXI::AXI_read_command);
trans.set_address(read_addr);
trans.set_data_length(16*4);
trans.set_data_ptr((unsigned char*)data);

found=axi_master_port.b_transport(trans);
```

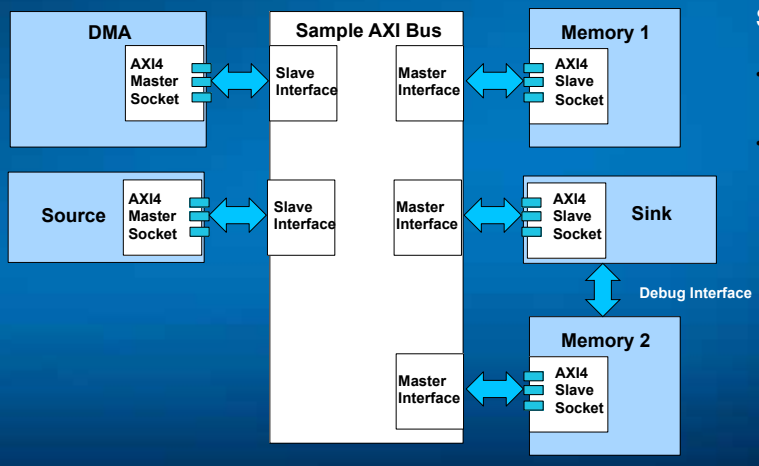

Master Socket Design
CIRCUIT SUTRA
THREADS
b_transport()
FIFO1
Mem_FIFO1
write resp signal
FIFO2
Mem_FIFO2
read resp signal
WA (cynw_p2p_direct_out)
WD (cynw_p2p_direct_out)
WR (cynw_p2p_direct_in)
RA (cynw_p2p_direct_out)
RD (cynw_p2p_direct_in)
AXI ports
AXI ports
AXI ports
AXI ports
AXI ports


Slave Socket Design
CIRCUIT SUTRA
AXI ports
AXI ports
AXI ports
AXI ports
AXI ports
WA (cynw_p2p_direct_out)
WD (cynw_p2p_direct_out)
WR (cynw_p2p_direct_in)
RA (cynw_p2p_direct_out)
RD (cynw_p2p_direct_in)
get()
get()
put()
get()
put()
bus_monitor _slave
CTHREAD
Write data to decoder of slave module
Read data from decoder of slave module

AXI protocol features

- Features Supported
  - All burst types INCR, FIXED,WRAP
  - Narrow transfers
  - Unaligned transfers
  - Setting strobes at master, checking strobes at slave during write
  - Variable data transfer size (AxSIZE)
  - Multiple outstanding transactions at slave, master
- Features not Supported
  - ACE protocol signals: AxCACHE, AxUSER, AxPROT,AxLOCK

Verification Setup



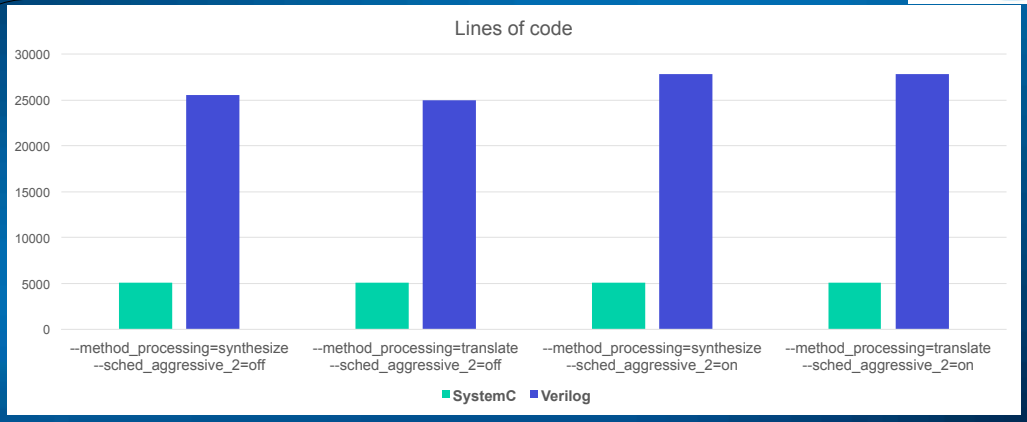
Same test suite used for:

- SystemC design (SystemC Simulator)
- Resultant Verilog design (Verilator + SystemC simulator)

Benefits

- Design productivity
  - Less amount of code
  - Less efforts for development & maintenance
  - Less probability of bugs
  - Same SystemC code can be used to generate the RTL for different applications
- Verification productivity
  - Bulk of functional verification can be done at behavioral level
  - Faster simulation results in faster verification
  - Less code results in fewer bugs related to functionality
- HLS Quick Start Package (QSP) for AMBA AXI
  - Re-usable master & slave sockets for designing AXI compliant IP blocks
  - Designers focus on functionality of their IP. Need not worry about implementing complex AXI protocol
  - IP designs are protocol independent. AXI sockets can be replaced by the sockets of other bus (eg.. OCP-IP)

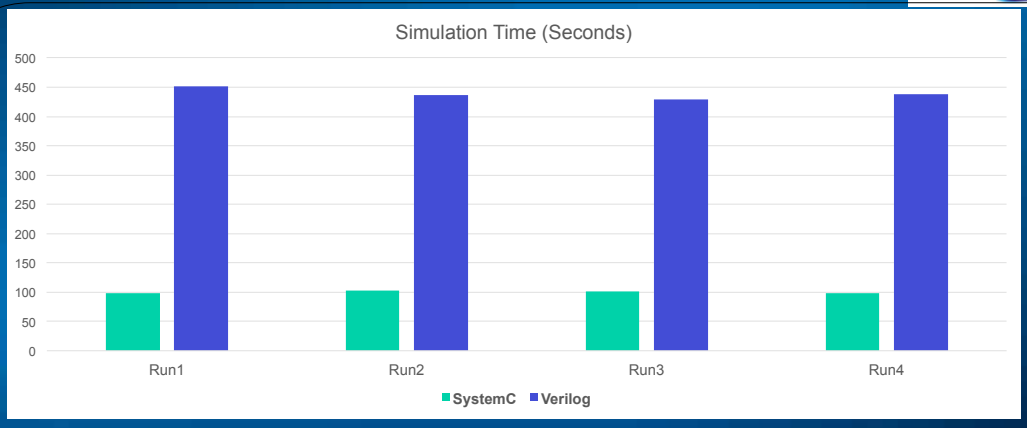
Smaller Code Size



More than 5x code size reduction

Further benefits can be realized by using same SystemC code to generate RTL for different applications

Faster Simulation



More than 4x faster simulation

Future Roadmap

- Integrate with UVM based verification flow
- Optimization
  - Optimize the code further for specific applications
- HLS-QSP
  - Add new portfolio of re-usable HLS models and modeling infrastructure
  - OCP-IP bus sockets
  - Hardware accelerators for widely used algorithms


CIRCUIT SUTRA
Transforming Semiconductors
Transforming Electronics
Thank You
www.circuitsutra.com/systemc_ip
info@circuitsutra.com