Welcome

Agenda

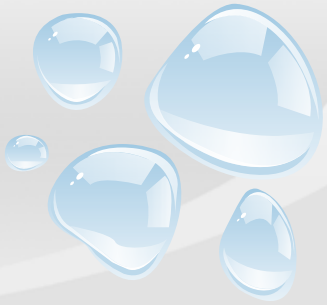
- About Accellera
- Current news
- Technical activities
- IEEE collaboration

accellera SYSTEMS INITIATIVE

Accellera Systems Initiative

Our Mission

- To provide design and verification standards required by systems, semiconductor, IP and design tool companies to enhance a front-end design automation process.
- To collaborate with its community of companies, individuals and organizations in delivering the standards that lower the cost to design commercial EDA, IC and embedded system solutions.



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Broad Industry Support

Corporate Members

AMD, ARM, Cadence, Ericsson, Freescale semiconductor, Intel, Mentor Graphics, NXP, Qualcomm, Sonics, ST, Synopsys, Texas Instruments

Associate Members

AGNISYS, ALDEC, Altera, Analog Devices, SPYGLASS, Boeing, Broadcom, Cisco, dialog, Doulos, Fraunhofer IIS, IBM, Imagination, JASPER design automation, magillem, NEC, NVIDIA, OFFIS, PARADIGM WORKS, Semifore, UPMC, XILINX

Welcome new members: Imagination Technologies, Analog Devices and Dialog Semiconductor!

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Global Presence

- DVCon USA March in Silicon Valley
- DAC June in San Francisco
- Japan Users Group July in Yokohama
- **DVCon India** September in Bangalore
- **DVCon Europe** October in Munich
- EDS Fair November, location TBA
- Accellera Day Taiwan December, location TBA

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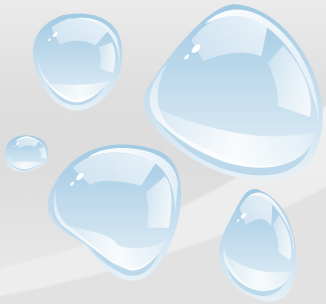

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DVCon Europe and DVCon India

www.dvcon-europe.org

- October 14-15, 2014
- Hilton Munich City, Germany
- Registration opens July 1

www.dvcon-india.org

- September 25-26, 2014
- Park Plaza, Bangalore, India
- Call for papers open June 1

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News & Events

- **October 2013**
  - Acquired Open Core Protocol Specification
- **February 2014**
  - Announced DVCon Europe, October 14-15, 2014 in Munich
- **March 2014**
  - Accellera Day at DVCon US
  - Andrew Goodrich Receives Technical Excellence Award
- **April 2014**
  - SystemC Core Language and Verification Libraries Released
  - ISCUG becomes DVCon India, to be held September 2014 in Bangalore
- **May 2014**
  - Yatin Trivedi Receives 2014 Accellera Leadership Award

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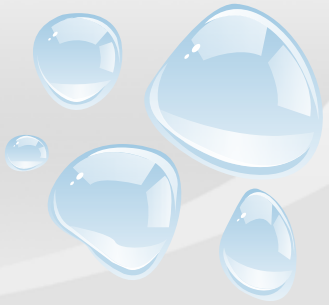

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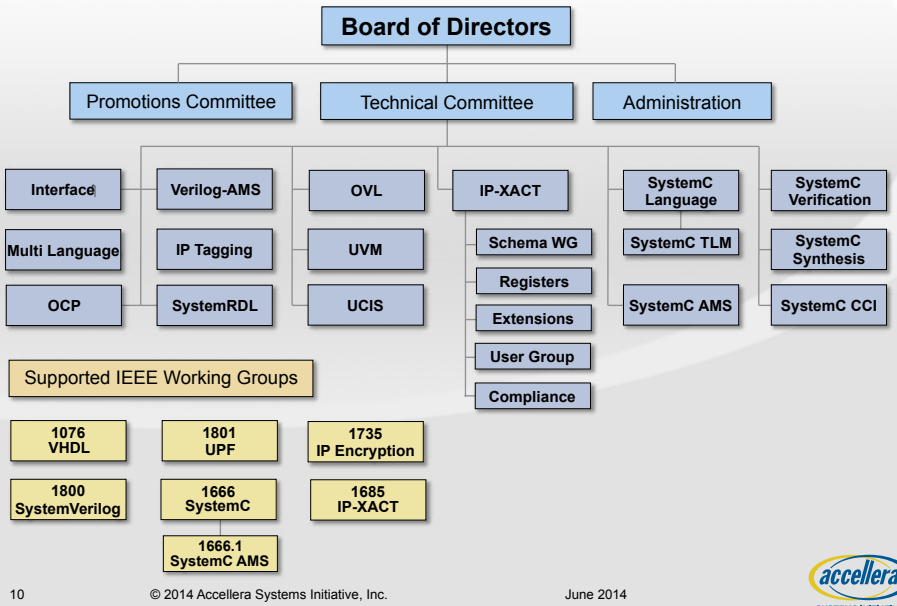

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Current Standards

- Intellectual Property (IP) Tagging 1.0
- IP-XACT - Update of IEEE 1685 and Vendor Extensions 1.0
- Multi-Language (launched)
- OpenCore Protocol (OCP) 3.0
- Open Verification Library (OVL) 2.8.1
- Standard Co-Emulation Modeling Interface (SCE-MI) 2.2
- SystemC Synthesizable Subset
- SystemC Analog Mixed-Signal (AMS) 2.0
- SystemC Configuration, Control & Inspection
- SystemC Language and Examples 2.3.1 (includes TLM 2.0)
- SystemRDL 1.0
- Unified Coverage Interoperability Standard (UCIS) 1.0
- Universal Verification Methodology (UVM) 1.1
- Verilog-AMS (V-AMS) 2.3.1
- Open Source Companions:
  - SystemC Proof of Concept Library (POCL)
  - SystemC Verification Library 2.0
  - UVM Reference Implementation 1.1d

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Ongoing Technical Activities

Upcoming Releases

IP-XACT - IEEE 1685-2009 Vendor Extensions 1.1	3rd Quarter 2014
Multi-Language – Initial release of POC (Skeleton)	3rd Quarter 2014
Standard Co-Emulation Modeling Interface (SCE-MI) 2.3	1st Quarter 2015
SystemC Synthesizable Subset 1.0	4th Quarter 2014
SystemC Analog Mixed-Signal (AMS) Users Guide 2.0	3rd Quarter 2014
SystemC Verification 1.0 & UVM SystemC 1.0	4th Quarter 2014
SystemRDL 2.0	1st Quarter 2015
Universal Verification Methodology (UVM) 1.2	2nd Quarter 2014
Verilog-AMS (V-AMS) 2.4	2nd Quarter 2014

DVCon – our flagship conference - now global!

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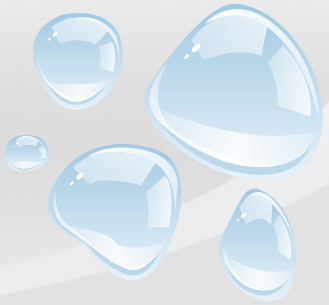

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Strong Partnership with IEEE

- IEEE Get program allows access to EDA & IP standards worldwide
  - IEEE 1666 SystemC
  - IEEE 1685 IP-XACT
  - IEEE 1800 SystemVerilog
  - IEEE 1801 Unified Power Format (UPF)
- Provide resources and infrastructure as needed to advance IEEE Standards Association Working Groups
  - 1076 VHDL
  - 1666 SystemC Language
  - 1666.1 SystemC AMS
  - 1685 IP-XACT
  - 1735 IP Encryption
  - 1800 SystemVerilog (SV)
  - 1801 Unified Power Format (UPF)

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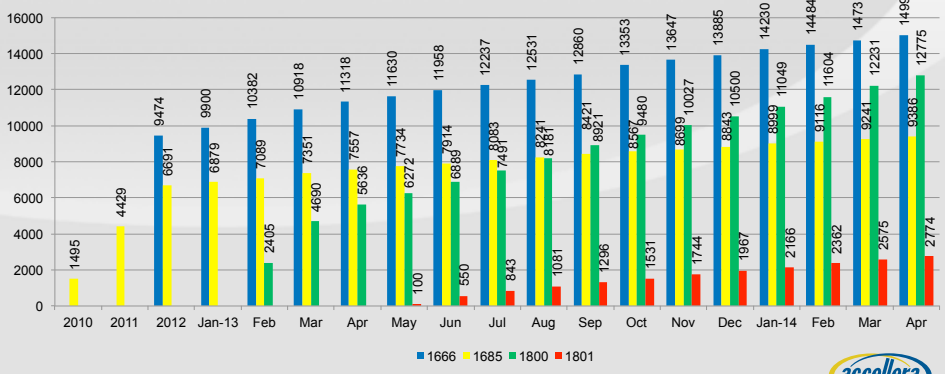
IEEE Standards Access at No Charge

- **Accellera Relationship with IEEE-SA**
- **Accellera may select up to 6 standards for "IEEE Get" program**
  - http://standards.ieee.org/about/get/

40,000 downloads!

Cumulative Downloads 2010-2014



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Advancing Standards Together

- **Share your experiences**
  - Visit www.accellera.org and use new UVM, OCP and SystemC Communities and register to post on forums
- **Show your support**
  - Record your adoption of standards
- **Become an Accellera member**
  - Join working groups

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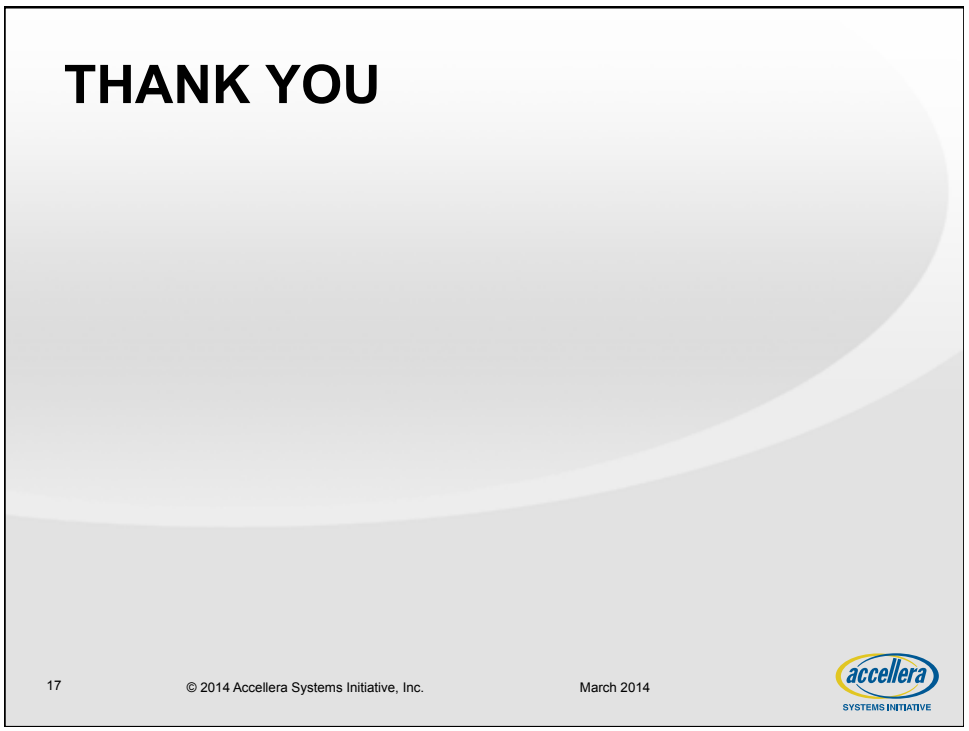
THANK YOU
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