



# **SystemC Enabling Embedded System Design at Sandia**

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Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company,  
for the United States Department of Energy's National Nuclear Security Administration  
under contract DE-AC04-94AL85000.





# **Sandia National Labs has 59**

**years of exceptional service in the National Interest**

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- **History**

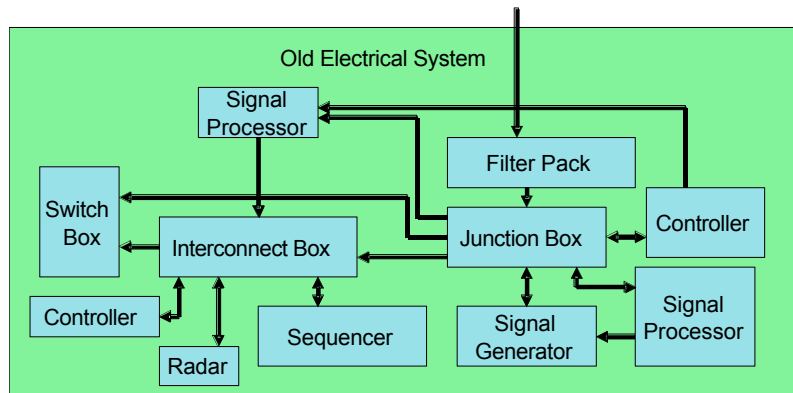
- **Formed to provide Engineering Support to Los Alamos NL**
- **Initially Formed as the Z-Division in 1945**
- **Renamed Sandia Corporation in 1949**
- **Became a National Laboratory in 1979**

- **Work**

- **Provide engineering support for Los Alamos and Lawrence Livermore National Labs**
- **Satellite and space applications**
- **Robotics research**
- **IC fabrication**
- **Leading research facility in MEMs devices**

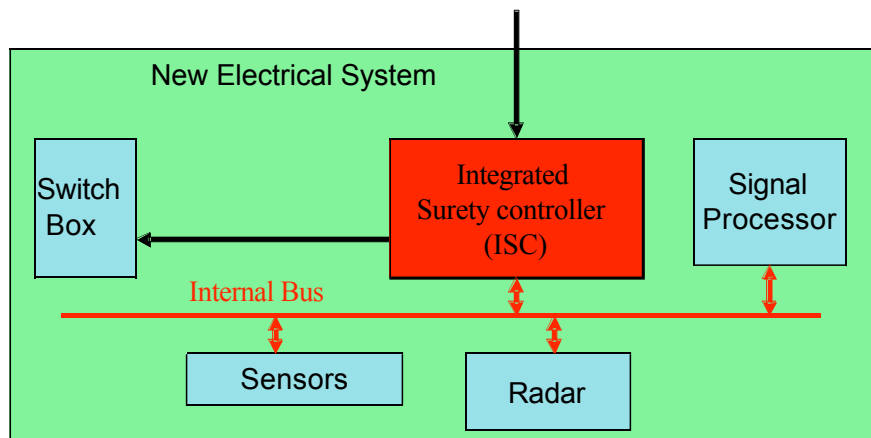


# A New Architecture for the Electrical System.



## Disadvantages of Current Architecture

- Many Electrical Components
- Lots Of Interconnect
- Difficult to add functionality



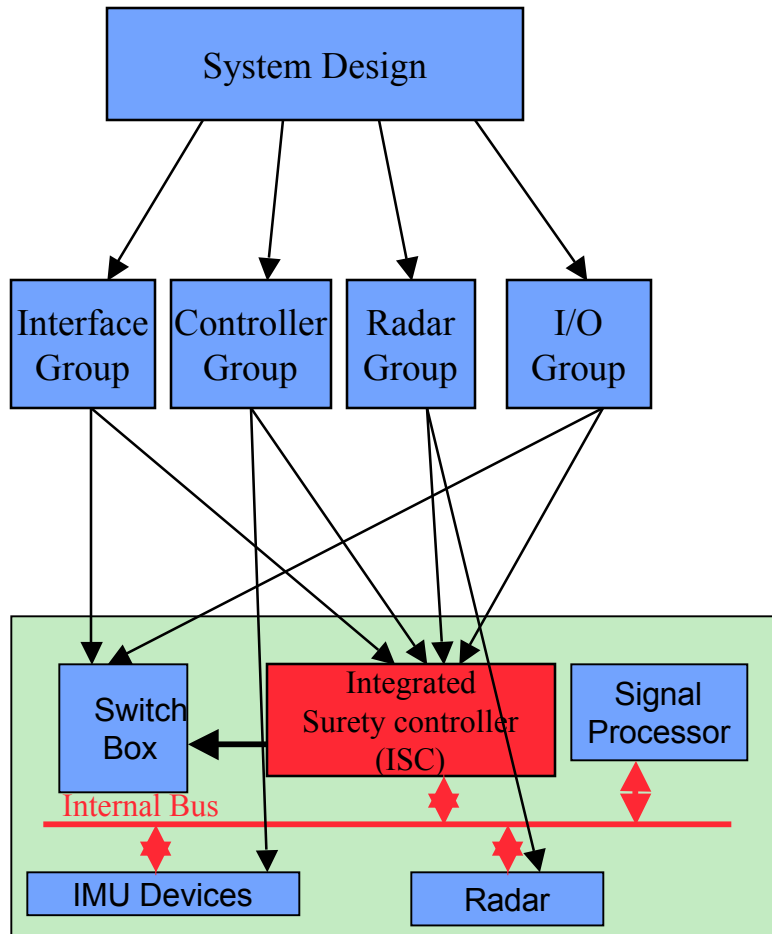
## Features of New Architecture

- Central controller
- Shared bus
- Improved surety
- New functionality
- Expandable/upgradeable

We are implementing the ISC in SystemC.



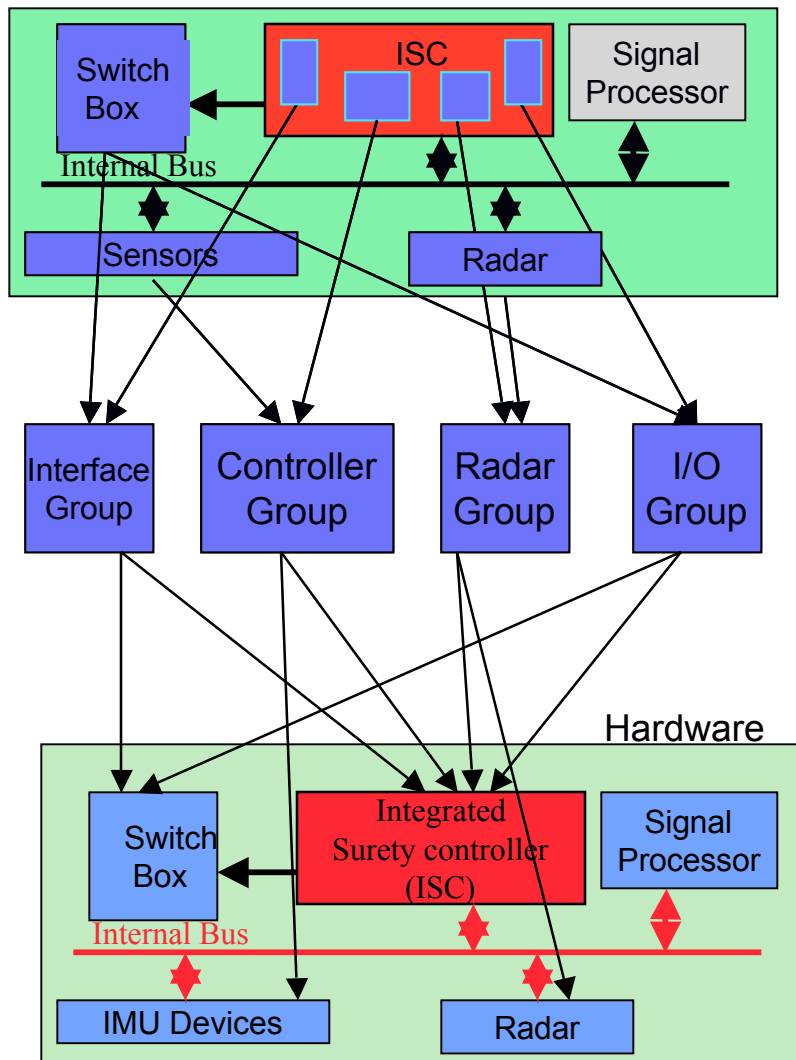
# The current design framework makes iterative improvements difficult.



1. Systems Group Defines Architecture
2. Written requirements given to individual component groups
3. Component groups create and test the hardware and software designs
4. Component designs given back to systems group
5. Component designs are fabricated and combined into final design and tested as a complete system



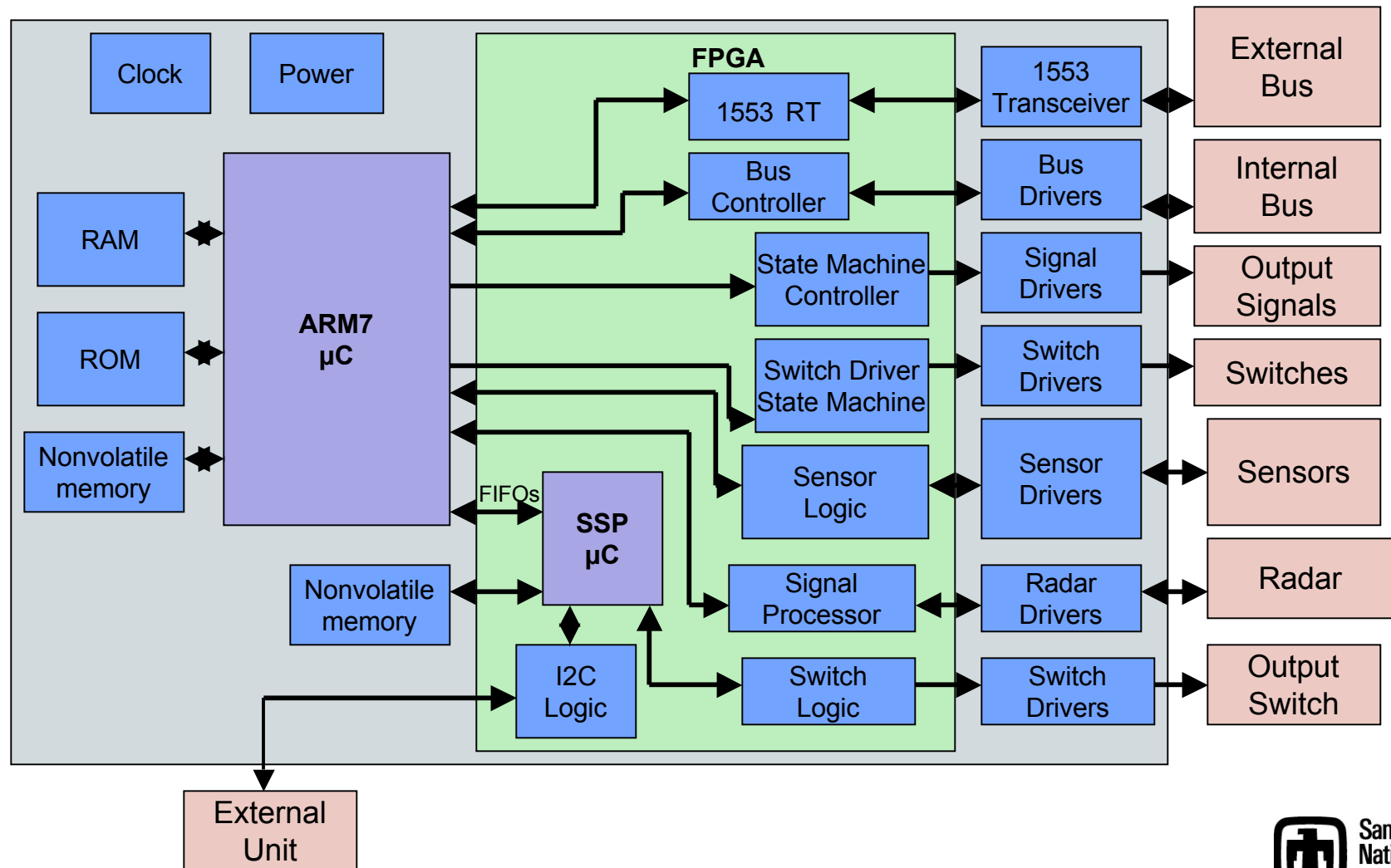
# Using SystemC for system level modeling.



1. Systems Group creates behavioral models of the System.
2. Component behavioral models become design specifications.
3. Component designs simulated in system model which is updated with latest component models.
4. System function is verified through simulation before hardware is built.



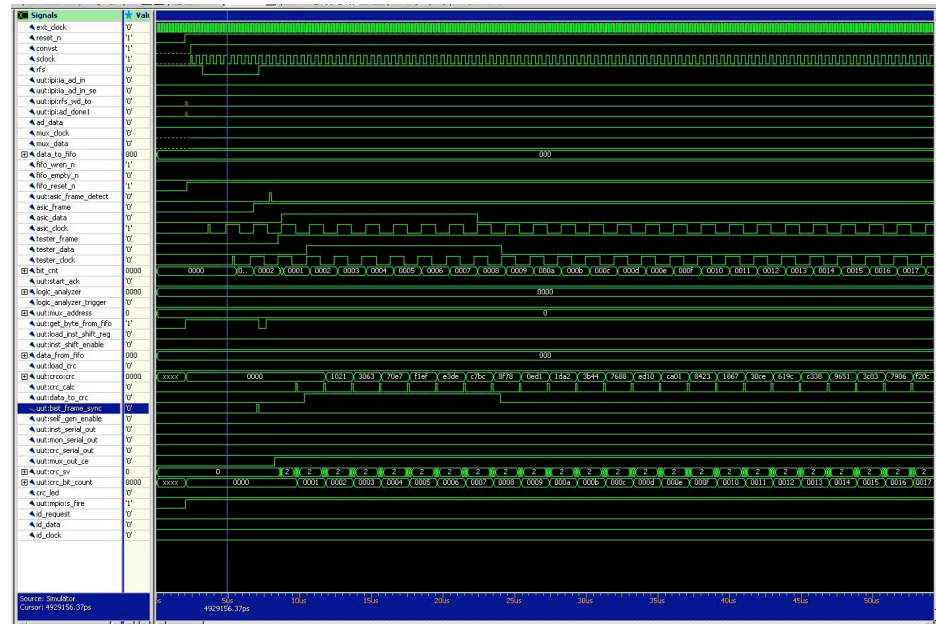
# ISC is the first development project to use the new architecture.





# SystemC offers many advantages in development of the ISC.

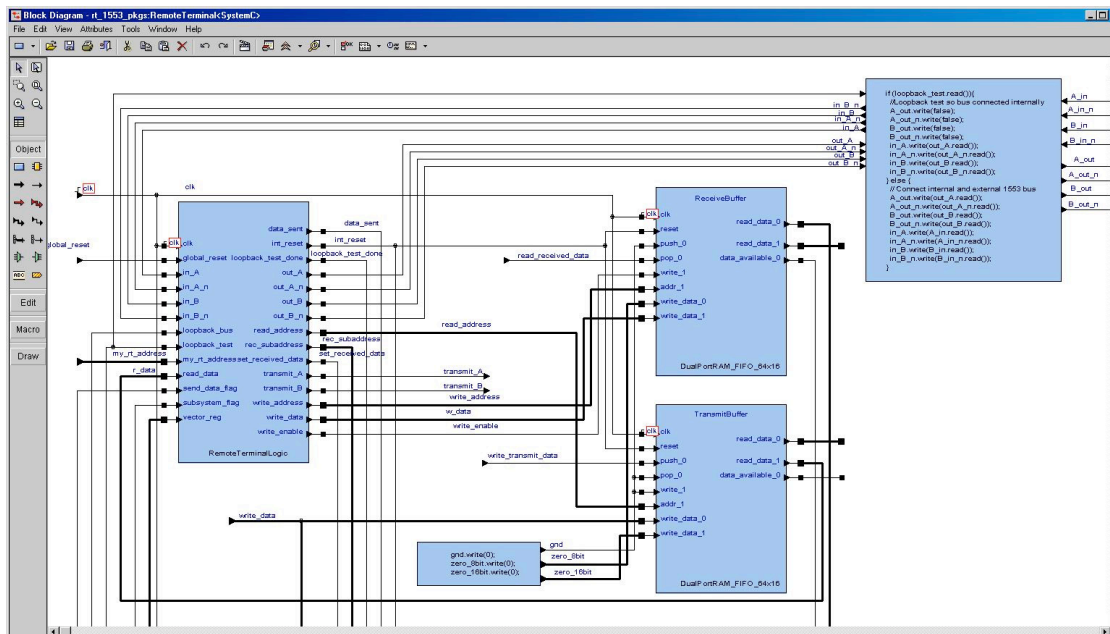
- HW/SW co-development
- Design collaboration during development
- Higher simulation speeds
- Flexible modeling/simulation options
- Complex mathematical algorithms





# Implementing the ISC in SystemC has been straight forward.

- Implementing functional blocks at the RTL level
- We used Summit's Visual Elite software
  - Summit's FastC simulator was used to ensure our SystemC HDL code was synthesizable.
  - Summit's (C2HDL) to create Verilog modules from our SystemC designs
  - The Verilog modules synthesized for Xilinx FPGA
- High level behavioral models were used for test benches

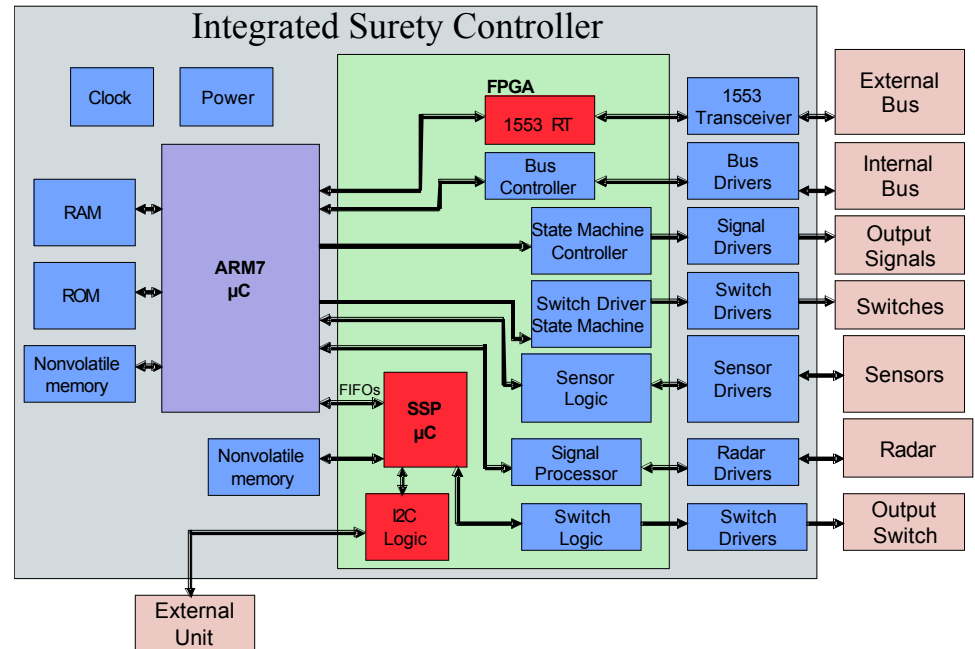







# Current State of the Project.

- We have created the ISC design with the Arm7, a VirtexII FPGA, and the other drivers and circuitry.
- We have implemented the SSP and the 1553 RT in SystemC
  - We have done SystemC simulations of these blocks.
  - We have synthesized the SystemC blocks and are testing them in hardware.
- We are currently deciding if we want to pursue implementing the design in SystemC or just use SystemC for architectural modeling



 => Blocks have been implemented in SystemC



## **SystemC has a lot to offer to the future of the ISC Project.**

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- **Purchase SystemC ARM7 simulation module**
  - **Co-simulate ARM7, SSP, and custom hardware**
- **Integrate high level Radar processing algorithms into design (MATLAB or C algorithms)**
- **Use SystemC to develop system architectural models**
  - **This could change the way system level designs are done at Sandia**



## **SystemC is changing the face of embedded system design.**

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- **“Interchangeable” behavioral and hardware models**
- **Greater collaboration across development groups**
- **Potential for modeling complete systems including digital, analog and mechanical elements.**
- **Potential for massively parallel processing to do detailed environmental response simulation.**
- **Potential for “free” SystemC simulators to facilitate gate level validation.**
- **Potential for entirely new synthesis paradigms.**