A SystemC Benchmark Suite for Evaluating MPSoC Tools and Methodologies

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<table>
<thead>
<tr>
<th>Feature</th>
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<tbody>
<tr>
<td>An open source scalable set of MPSoCs, with 1 up to 64 cores</td>
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<td>Four different processor models: ARM, PowerPC, SPARC, and MIPS</td>
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<td>Ips, Interconnection and devices using TLM 2.0</td>
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<td>Power Characterization for MIPS and SPARC</td>
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<td>Two different abstraction levels</td>
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<td>13 parallel application, including a POSIX thread emulation library</td>
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<td>844 configurations – automated by scripts</td>
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http://archc.org/benchs/mpsocbencb/
Outline

- Motivations and Goals
- Simulation Infrastructure
- How to use the benchmark
- Characterization
Motivation

The complexity of Multiprocessor System-on-Chip (MPSoC) designs forces designers into an even higher level design methodology.

Credits:
http://www.sonymobile.com/br/products/phones/xperia-play/
Motivation

- **New Challenges**
  - ✔ The adoption of Multiprocessor System-on-Chip (MPSoCs) in the embedded systems state of the art
  - ✔ Hardware & Software

- **Design Productivity**
  - ✔ By providing a software development platform before the final MPSoC architecture details are fixed

- **Requirements**
  - ✔ The lack of a benchmark suite to assist validation and evaluation of new techniques and tools causes delays in the development tools life cycle.
Our Goal is ...

... to provide a complete SystemC simulation infrastructure in a hardware/software multiprocessor environment in order to facilitate the deployment, analysis, and verification of new concepts, new tools, and methodologies in MPSoC designs.
Infrastructure

- 1, 2, 4, 8, 16, 32, or 64 cores
- A 512MB shared memory
- A hardware lock device
- Different interconnections
ArchC is a SystemC-based Architecture Description Language
MIPS and SPARC include Power Consumption Estimates
Design using a Router

Loosely Timed

- The communication is achieved by TLM 2 blocking transport interface with timing annotation
Design using a NoC

- Mesh based NoC using XY routing protocol
- NoC is totally configurable in runtime through user parameters
- Different approaches:
  - NoC-LT: Loosely Timed
  - NoC-AT: Approximately timed

Ni,j: noc nodes
W: wrappers
P: processors or IPs
13 Parallel Applications

- 7 From ParMiBench
- 4 From SPLASH-2
- 1 Multisoftware Application composed of 16 single-core programs from Mibench
- 1 Multisoftware Parallel Applications composed of 4 applications from ParMiBench combined in different multithreaded versions (1-thread, 2-threads, 4-threads, 8-threads, and 16-threads each)
How To Use

./mpsocbench <arguments>

$ ./mpsocbench -r -s fft -p mips -pw -n 64 -i noc -t LT

Build and run
Software
FFT
64-mips platforms
With power consumption
Using NOC-LT

$ ./mpsocbench -b -s all -p all -n 16 -i router

Build
All
All 16-core
Platforms (with all
processor models)
Using router
(without running)
(default LT)
How To Use

./mpsocbench <arguments>

$ ./mpsocbench -b -s all -p all -n all -i all -c

build

all software

all platforms

all interconnection

enabling execution in a condor cluster

This command line will create a directory for each platform, including all executable files and input files required for parallel execution on a cluster.
Number of Instructions executed in single-core platforms using the four processor models

Applications with a lower computational load

Applications with a higher computational load
Number of lock accesses
All processors – 1 to 64 cores

Platforms

Number of Locks accesses (in millions)

Number of lock accesses

MPSoC Bench
Benchmark Suite

stringsearch
sha
Simulation Time

Comparison among Router, NOC-LT, and NOC-AT

Multi-PowerPC running Dijkstra using Router, NOC-LT, and NOC-AT as interconnection device
Power measurements
Dual-mips running FFT
Power measurements
Quad mips running Basicmath

![Graph showing power measurements for mips1, mips2, mips3, and mips4 over time.](image-url)
Conclusions

• We've proposed the MPSoCBench, an open-source benchmark composed of a scalable, configurable and extensible set of MPSoCs

• Available in two ways:
  • a virtual machine with all infrastructure ready for use;
  • a source code

Ready for your research and evaluation!

The benchmark and tutorials at:
http://archc.org/benchs/mpsocbench/
Thank you!
Do you have any questions?

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