Hybrid Simulation of Digital and Analog model using SystemC and SystemC AMS/Verilog AMS

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Key Objective

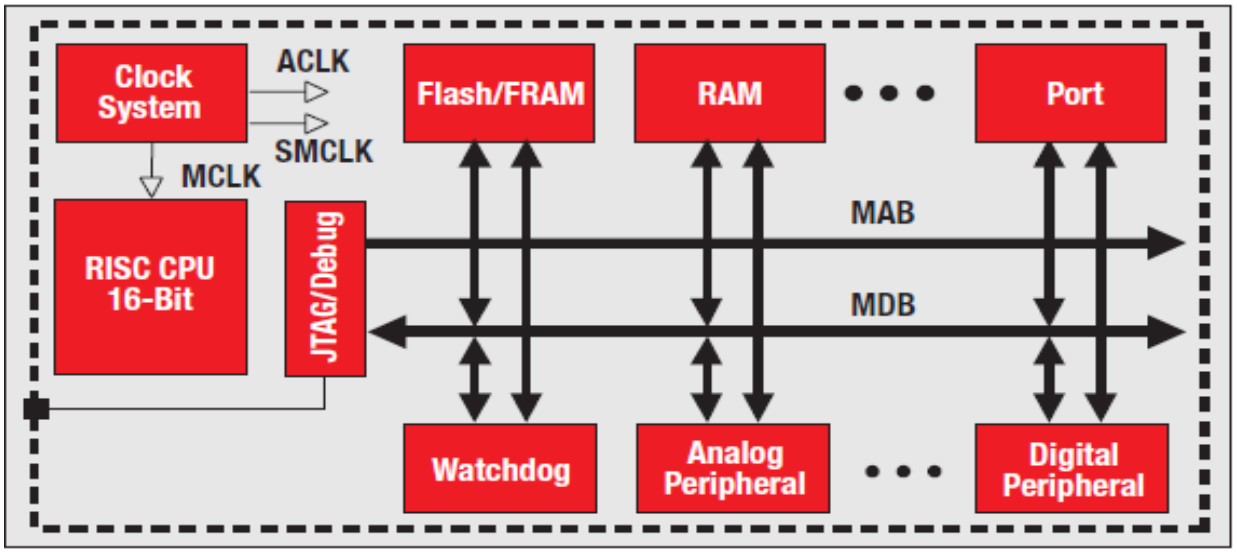
The paper talks about study done within TI to understand the challenges behind setting up a simulation framework for mixed simulation processor. A mixed-signal integrated circuit is any integrated circuit that has both analog circuits and digital circuits on a single semiconductor die

Key Objective:

- To setup a flow within TI for Digital and Analog co-simulation using services of SystemC, SystemC-AMS and Verilog AMS.
- Look into feasibility and identify the challenges for simulating a mixed signal processor like TI's MSP430 microcontroller which contain both digital and analog components

Brief Summary on how the project scope was defined

- Started with defining key IP's to be modeled for a typical Mixed signal processor like TI MSP430 (used for Motor Control, Data logging, etc.)



- The Analog Peripheral includes DAC12, ADC12, Comparator, RF Front End ….
- The project scope was reduced to
  - Simple traffic model, sending bit stream, representing the Digital world
  - Simple DAC model to represent the Analog component

Brief Summary on Different Phases

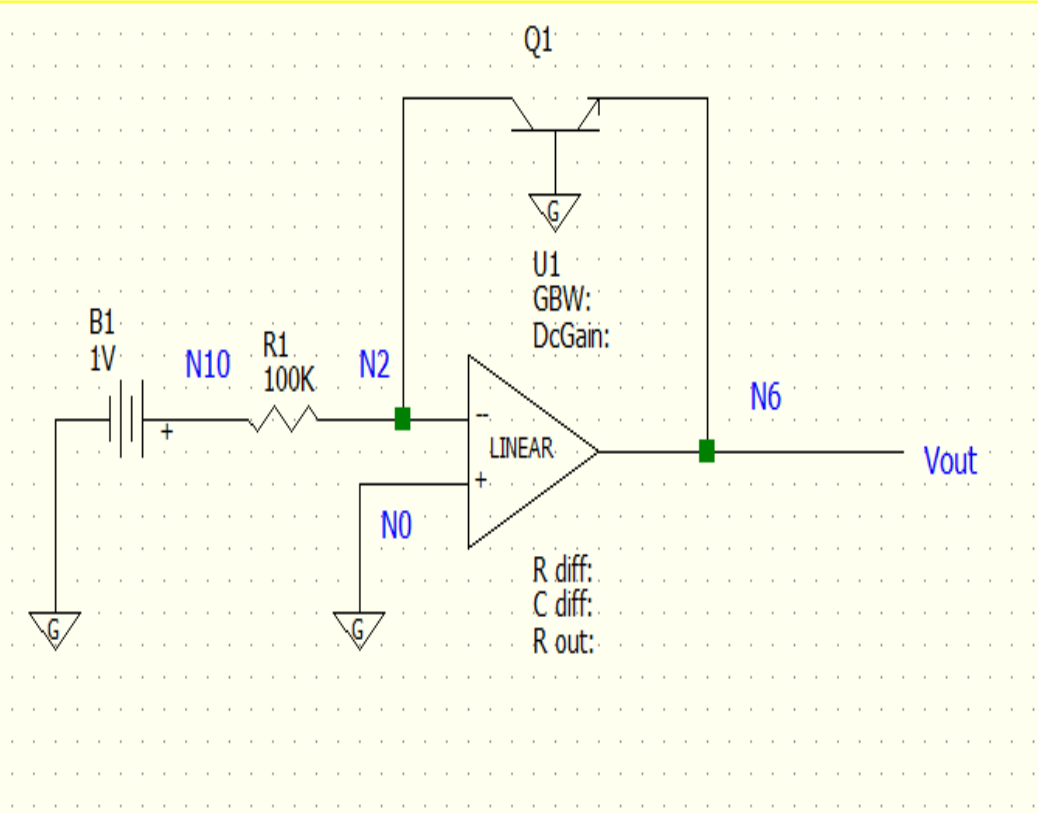
The entire project spanned across three phases:

- Phase 1 : Develop Logarithmic Amplifier analog model using Spice and compare with SystemC AMS
  - The intend of this phase was to compare Spice modeling with SystemC AMS/Verilog AMS
- Phase 2 : SystemC - TLM - SystemC AMS co-simulation
- Phase 3 : SystemC - TLM – Verilog AMS co-simulation

PSpice – Example

- Logarithmic Amplifier. The below equation defines the behavior of the model

$$Vout = - kT/q * \ln (Vi / Is*R1)$$



Assignment 1 Q-5.
VCC 7 0 12
VEE 0 4 12
VI 10 0 DC 1
R1 2 10 100K
X1 0 2 7 4 6 UA741
Q1 2 0 6 Qmod
.MODEL Qmod NPN (IS=4E-14
BF=175)
.lib "eval.lib"
.DC VI 1 10 1m
.PROBE
.END

PSpice vs SystemC AMS

- PSPICE
  - Pros
    1. Inbuilt model definitions of majorly all Analog components available in market today
  - Cons
    1. Lower level of abstraction
    2. Very long simulation times
    3. Interfacing with Digital simulation could be a challenge here
- SystemC AMS
  - Pros
    1. Higher level of abstraction
    2. Capabilities for Descriptive as well as behavioral modeling of analog circuits
    3. Faster simulations
    4. Easily integrated with SystemC, C++ models
  - Cons
    1. Not always feasible to determine the exact behavior of an Analog circuit
    2. Small number of pre-defined Electrical elements

Why SystemC AMS / Verilog AMS over Spice for Co-simulation with SystemC

- Behavioral modeling instead of transistor level design
- Support different levels of abstraction
- Very fast simulation speed
- Possible to verify entire system model instead of individual Spice blocks

Phase 2 : SystemC –TLM –SystemC AMS

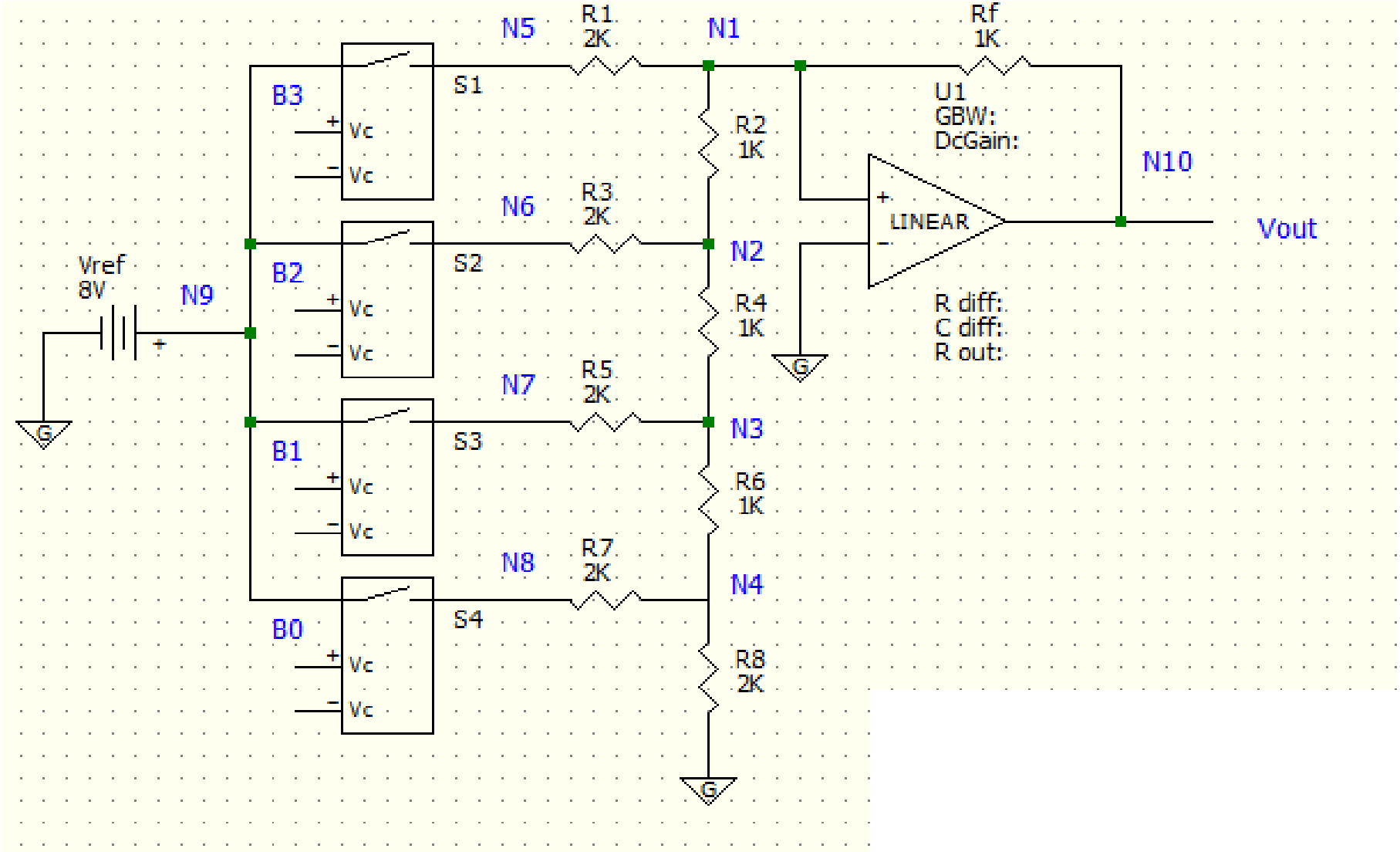
- SystemC “ MASTER “ module generating 4-bit Digital data streams
- At every positive edge of clock , a “ Blocking Transport “ call is placed by the master to the “ SLAVE “ module
- The “ SLAVE “ module accepts the “ Blocking Transport “ call and retrieves “ Memory Address “ and “ 4-bit Data “ from the “ Transaction Object “.
- The 4-bit Digital data is used as the control logic for an 4-bit Digital-to-Analog Convertor modeled using SystemC-AMS.
  - An R-2R ladder based Digital to Analog convertor modeled in SystemC AMS using its three different modeling techniques viz.
    1. Timed Data Flow Modeling (TDF)
    2. Linear Signal Flow Modeling (LSF)
    3. Electrical Linear Network Modeling (ELN)

A Brief comparison on various SystemC AMS Model of Computation

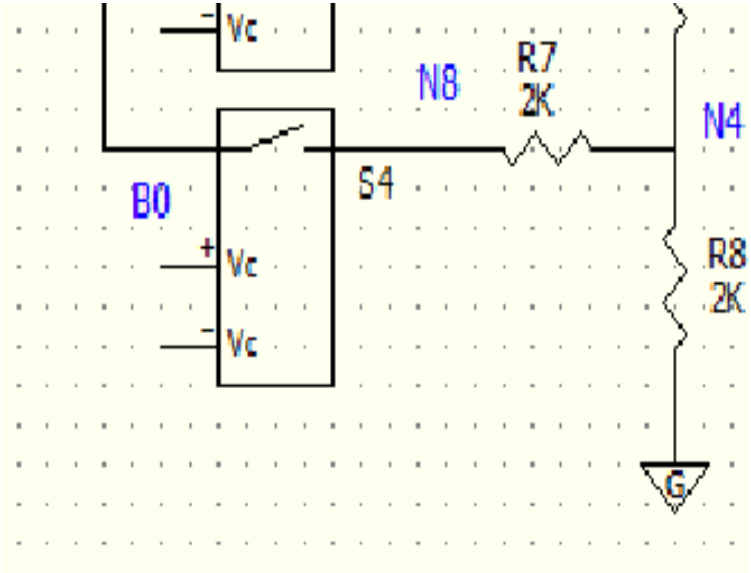
	Descriptions	Transactions/sec
TDF	• TDF model composed of sets of connected TDF modules • Each TDF module contains – Output ports and input ports – C++ method that computes a mathematical function. • The overall behavior of the cluster is therefore defined as the mathematical composition of the functions of the involved TDF modules in the appropriate order	~2850
LSF	• An LSF model is composed of a set of connected LSF modules, which will form together an LSF equation system or LSF cluster. • Allows the modeling of AMS behavior defined as relations between variables of a set of linear algebraic equations. • An example block is shown in the next slide	~1666
ELN	• An ELN model uses electrical primitives and their interconnections to model conservative, continuous-time	~1000

Note : The rest of the paper would take ELN DAC example for SystemC AMS

Design for 4-bit R-2R Ladder DAC



Code Snippet for the DAC in SystemC-AMS(ELN)




```
.....................................
sca_eln::sca_de::sca_rswitch S4,.......;
sca_eln::sca_r R0,……
sca_eln::sca_node N1,N2,N3,N4,N5,N6,N8,N9,....,;
sca_eln::sca_de::sca_vsink v_out;
SC_CTOR(Memory) :
  socket("socket"),v_ref("v_ref",8,8,8..
{
  // Socket to interface with the digital world
  socket.register_b_transport(this,
&Memory::b_transport);
  S4.p(N9);
  S4.n(N8);
  S4.ctrl(B[0]);
  R7.p(N8);
  R7.n(N4);
  ..........................
}
```

Phase 2 : SystemC - TLM - Verilog AMS

- SystemC “ MASTER “ module generating 4-bit Digital data streams
- At every positive edge of clock , a “ Blocking Transport “ call is placed by the master to the “ SLAVE “ module
- The “ SLAVE “ module accepts the “ Blocking Transport “ call and retrieves “ Memory Address “ and “ 4-bit Data “ from the “ Transaction Object “.
- The Slave module talks to SystemC-Verilog AMS wrapper module.
  - This wrapper module is a special class of SystemC modules that facilitate conversion of SystemC data into a type as understood by Verilog AMS at the time of elaboration thus facilitating the linking of two different modeling standards.
- The 4-bit Digital data is used as the control logic for an 4-bit Digital-to-Analog Convertor modeled using Verilog AMS.

NOTE : The voltage out from the DAC can act as the interconnect port for connecting to any subsequent system blocks in the Analog domain**.**

SystemC-Verilog AMS Wrapper module example

```
/* SystemC module with interface with Verilog
    AMS */
#include"tlm_implementation.h"
class wrapper : public ncsc_foreign_module {
public:
sc_in<bool> in1;
sc_in<bool> in2;
sc_in<bool> in3;
sc_in<bool> in4;
sc_in<bool> clock;
wrapper(sc_module_name nm) :
    ncsc_foreign_module(nm),in1("in1"),in2("in2"),in3("i
    n3"),in4("in4"),clock("clock")
 {}
const char* hdl_name() const { return "wrapper"; }
};
```

```
/* Verilog AMS with interface with SystemC */
`timescale 1ns/1ps
`include "disciplines.vams"
module wrapper(in1,in2,in3,in4clock);
input in1,in2,in3,in4,clock;
ideal_dac dac(in1,in2,in3,in4,clock);
begin
always @(posedge clock)
$display("Data : ",in1,in2,in3,in4);
end
endmodule
```

Verilog AMS vs SystemC AMS

- Verilog AMS
  - Pros
    - Inbuilt model definitions of majorly all Analog components available in market today
    - More industrially accepted and used
  - Cons
    - Co-simulation not supported by many existing EDA tools. Those which support the same are extremely costly and only available as proprietary software

- SystemC AMS
  - Pros
    - Can be simulate with no EDA tools needed
  - Cons
    - Small number of pre-defined Electrical elements
    - Relatively new Analog modeling standard having it's first release as a standard less than a year ago. Thus, it is not extensively used inside of TI so far

Simulation speed for two cases

- SystemC-SystemC AMS
  - 100000 Transaction was processed in ~100sec, approx 1000T/per sec for ELN
  - Used Electrical Linear Network Modeling.

- SystemC – Verilog AMS
  - 100000 Transaction in 20 sec, approx 5000T/per sec
  - Used Algorithmic descriptions of transfer functions. This could explain the faster simulation speed compare to SystemC AMS ELN.
  - The speed is still higher than SystemC AMS TDF model (~2850 T/sec) which represent model in transfer function. Would need to investigate this difference.

Conclusion

- SystemC AMS and Verilog AMS do provide infrastructure to support mixed signal processor simulation. There are few challenges as mentioned below which need to be overcome.
  - SystemC – SystemC AMS provides a tool independent flow for mixed simulation. But SystemC AMS need to be more popular and adapted by industry. Again need to support more analog components.
  - SystemC- Verilog AMS solution dependents on EDA tools and this restrict free simulation

- Next step beyond this
  - Use the above study to do a Simulation of MSP430 Mixed signal processor.
  - Looks very much feasible , but again need to do more complex analog IP other than DAC. This could be a challenge in SystemC AMS and Verilog AMS

References

- **SystemC Reference Manual - http://homes.dsi.unimi.it/~pedersini/AD/SystemC_v201_LRM.pdf**
- **Verilog AMS Reference Manual - http://www.eda.org/verilog-ams/htmlpages/public-docs/lrm/VerilogA/verilog-a-lrm-1-0.pdf**
- **Cadence AMS Design Simulator - http://www.cadence.com/rl/Resources/datasheets/virtuoso_mmsim.pdf#page=10**