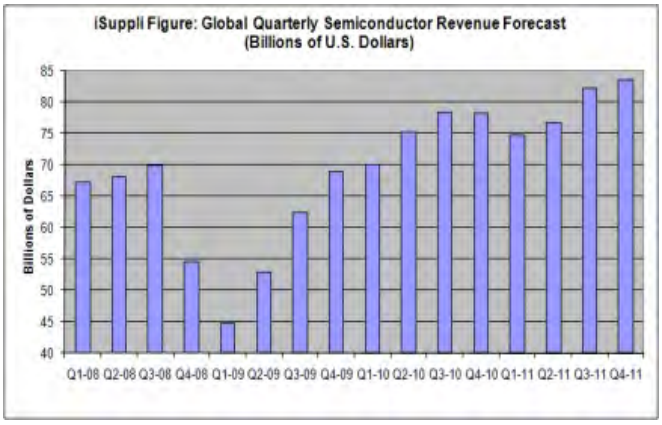
DVCON 2011
Navigating the SoC Era

Jim Hogan February 2011

Semiconductor Industry Forecast Projections
2010: ~30% 2011: ~10%



SIA
- -2010 f: $301B (33% growth)
- -2011 f: $319B (6% growth)
- -2012 f: $330B (3% CAGR)

IC Insights:
- -2010 f: $296B (31% growth)
- -2011 f: $329B (11% growth)
- -2012 f: $362B (10% growth)

Source: iSuppli

System on Chips (SoCs) Enable Innovation

Today's SoC – Not just an IC business any longer

- **SoCs increase semiconductor gross margins**
  - SoC margins: 40 - 60% vs. Discrete IC margins: 10 - 20%
- **SoCs are non-processors centric: Multi-CPU, multi-core, DSP cores, HW accelerators**
  - Differentiate through peripherals and software
  - Non-uniform and/or distributed memory architecture
  - ARM dominates mobile market, moving into servers
  - Windows support for ARM, breaks WIntel franchise
  - Intel ATOM must displace ARM, integrate into heterogeneous ARM/Intel SoCs
  - MIPS positioning as Android processor **CPU + FPGA, CPU + GPU …**
  - nVidia positioning as SoC block
- **Heterogeneous configurable compute fabrics (FPGA):**
  - Reference boards, prototyping, application software development …
  - Simulation acceleration, emulation, SoC debug …
- **SoC Always Optimization for Power, Performance, and Area/Cost**

1H 2010 Semiconductor Leaders – ARM processors have won the war

1H10 Top 20 Semiconductor Sales Leaders ($M)

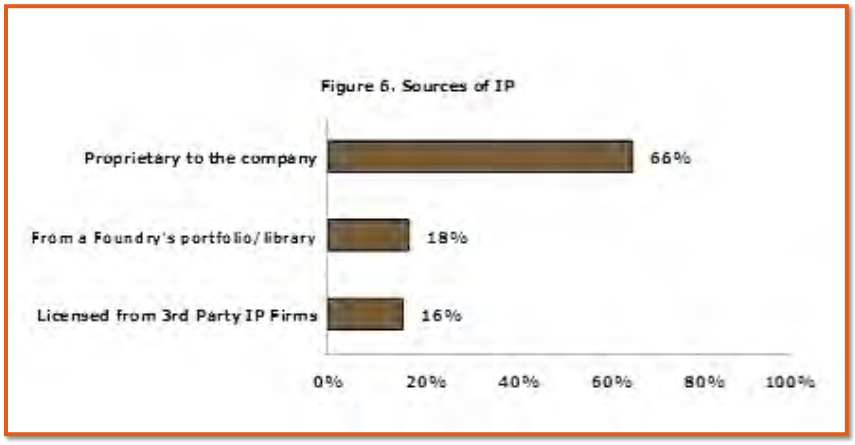
ARM Licensees

1H10 Rank	2009 Rank	Company	Headquarters	2009 Tot Semi	1Q10 Tot Semi	2Q10 Tot Semi	2Q/1Q % Change	1H10 Tot Semi
1	1	Intel	U.S.	32,325	9,485	9,910	4%	19,395
2 ★	2	Samsung	South Korea	21,273	7,137	8,159	14%	15,296
3 ★	3	TI	U.S.	9,697	2,990	3,262	9%	6,252
4 ★	5	Toshiba	Japan	9,537	3,240	3,002	-7%	6,242
5	6	TSMC**	Taiwan	8,989	2,885	3,293	14%	6,178
6	4	Renesas Electronics*	Japan	9,649	2,787	2,821	1%	5,608
7 ★	9	Hynix	South Korea	6,320	2,455	2,807	14%	5,262
8	7	ST	Europe	8,466	2,311	2,507	8%	4,818
9	10	Micron	U.S.	5,450	2,077	2,365	14%	4,442
10 ★	15	Elpida	Japan	3,948	1,625	1,913	18%	3,538
11 ★	8	Qualcomm***	U.S.	6,409	1,537	1,691	10%	3,228
12 ★	11	AMD***	U.S.	5,403	1,574	1,653	5%	3,227
13 ★	13	Infineon	Europe	4,617	1,438	1,540	7%	2,978
14 ★	14	Broadcom***	U.S.	4,271	1,404	1,547	10%	2,951
15 ★	12	Sony	Japan	5,245	1,300	1,248	-4%	2,548
16 ★	16	NXP	Europe	3,547	1,079	1,105	2%	2,184
17	19	Freescale	U.S.	3,302	972	1,056	9%	2,028
18	24	UMC**	Japan	2,815	935	1,043	12%	1,978
19 ★	17	MediaTek***	Taiwan	3,500	1,024	940	-8%	1,964
20	18	Fujitsu	Japan	3,377	955	933	-2%	1,888
—	—	Total	—	158,140	49,210	52,795	7%	102,005

*The merged entity of Renesas and NEC **Foundry ***Fabless

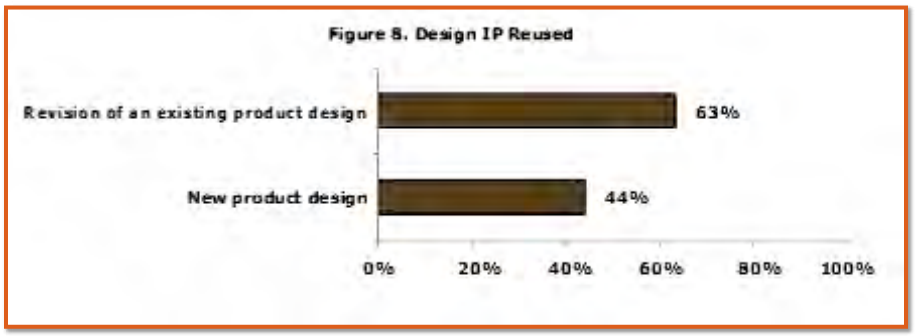
Source: IC Insights, company reports

IP is Integral Part of SOC



Source: 2010 Wharton-GSA Semiconductor Ecosystem Survey – Sources of IP

Surprisingly Large Portion of SOC is New IP



Source: 2010 Wharton-GSA Semiconductor Ecosystem Survey – Sources of IP

Practical Concerns for today's SOC Design Teams

Assembly and Management prior to Silicon Realization

- Diverse IP sources (internal and external)
- Driven from IP vendor directories
- Controlled access to IP data
- Ensure IP's lib/lef are compatible with your design environment
- Constraints for hard and soft IP
- IP usage tracking

Practical Concerns for today's SOC Design Teams
Verification prior to Silicon Realization

- Validate IP quality and functionality
  - Does it work?
    - Functionally, operationally, interactively
    - Cycle-based model extracted into IC model
  - Does it work with your design specification?
    - Can you write to the pins?
  - Does it work in your derivative designs?
- Derivative designs further complication
  - Bug traceability. Must find original instance
  - Must propagate changes through all revisions/derivatives

Source: Blind anonymous survey by IC Manage. 426 respondents

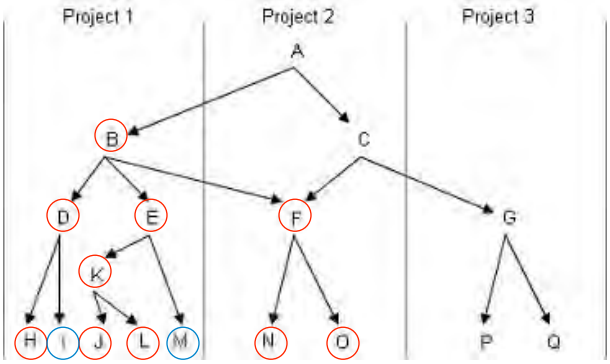
- 47% of engineering management cited project/tapeout delays due to DM issues
- 30% of organizations had commercial DM in early 2010

Data Explosion & IP are impacting Verification

For derivative tree below, if you find a bug in L and M, **how many releases are at risk?**

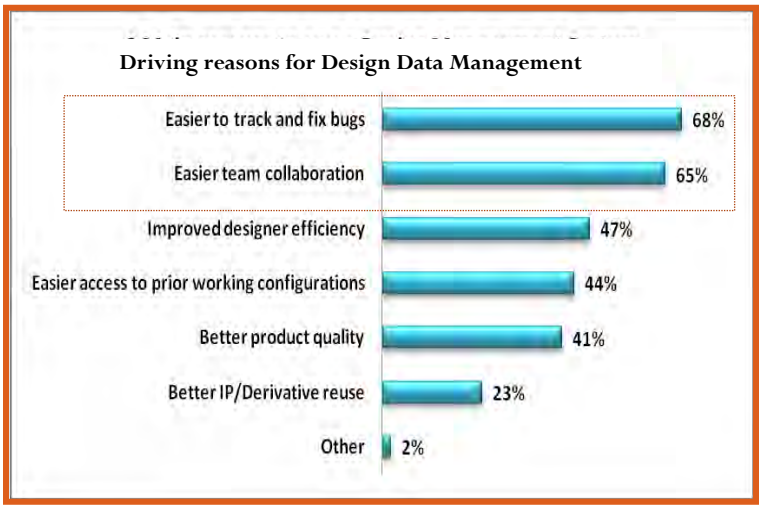
- The defect originated in a common ancestor of I and M.
- All descendants of the common release are potentially at risk.

Answer: 12



Source: IC Manage DDM quiz 2011

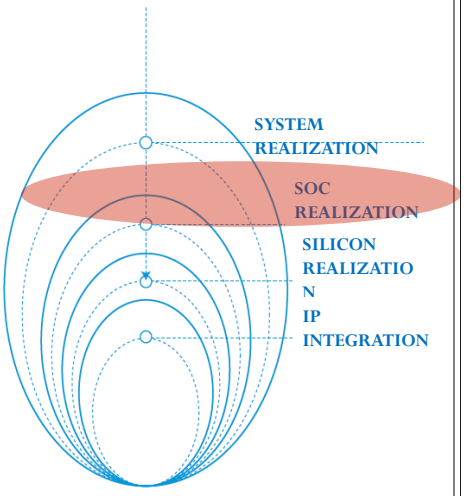
Verification & Interdependencies drive SOC Design Management



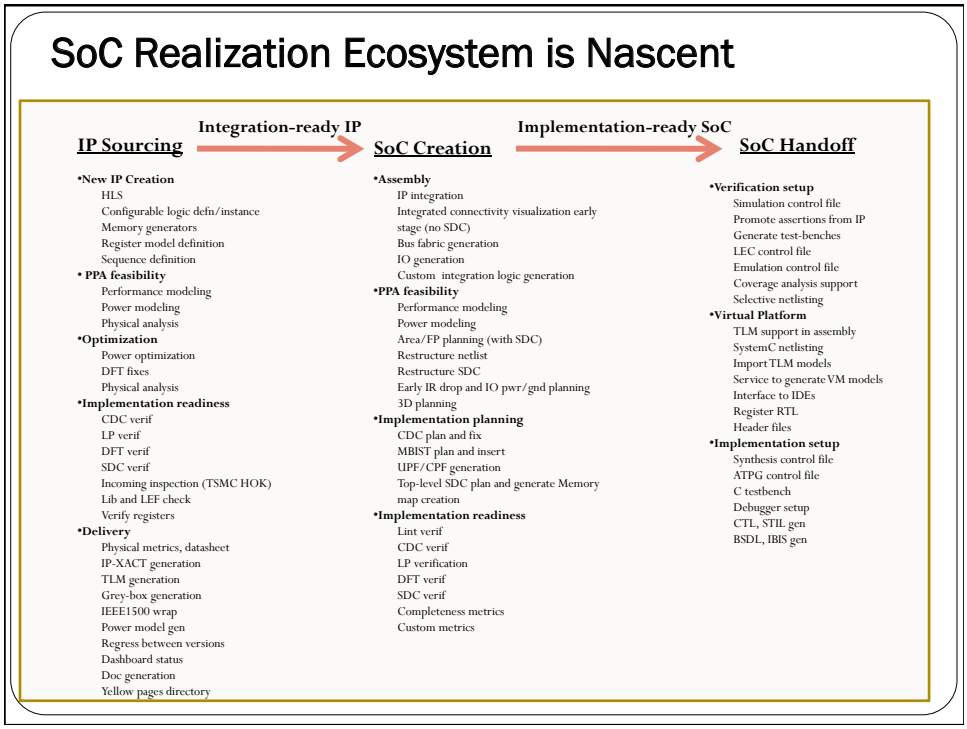
Source: Blind anonymous survey by IC Manage. 426 respondents

EDA360 Explored: SoC Realization

- **SoC realization is architecting individual SoC**
  - IP selection and management
  - Design assembly
  - Feasibility check (PPA)
  - Bare-metal software development
- **SoC realization requires**
  - Design data management
    - Assembly, Verification
  - Debug and analysis tools
  - Software models of specific SoC IP components/block ,e.g. processors,
  - Memory and controllers…



Source: Cadence Design Systems 2010


SoC Realization Ecosystem is Nascent
IP Sourcing
Integration-ready IP
SoC Creation
Implementation-ready SoC
SoC Handoff
•New IP Creation
HLS
Configurable logic defn/instance
Memory generators
Register model definition
Sequence definition
• PPA feasibility
Performance modeling
Power modeling
Physical analysis
•Optimization
Power optimization
DFT fixes
Physical analysis
•Implementation readiness
CDC verif
LP verif
DFT verif
SDC verif
Incoming inspection (TSMC HOK)
Lib and LEF check
Verify registers
•Delivery
Physical metrics, datasheet
IP-XACT generation
TLM generation
Grey-box generation
IEEE1500 wrap
Power model gen
Regress between versions
Dashboard status
Doc generation
Yellow pages directory
•Assembly
IP integration
Integrated connectivity visualization early stage (no SDC)
Bus fabric generation
IO generation
Custom integration logic generation
•PPA feasibility
Performance modeling
Power modeling
Area/FP planning (with SDC)
Restructure netlist
Restructure SDC
Early IR drop and IO pwr/gnd planning
3D planning
•Implementation planning
CDC plan and fix
MBIST plan and insert
UPF/CPF generation
Top-level SDC plan and generate Memory map creation
•Implementation readiness
Lint verif
CDC verif
LP verification
DFT verif
SDC verif
Completeness metrics
Custom metrics
•Verification setup
Simulation control file
Promote assertions from IP
Generate test-benches
LEC control file
Emulation control file
Coverage analysis support
Selective netlisting
•Virtual Platform
TLM support in assembly
SystemC netlisting
Import TLM models
Service to generate VM models
Interface to IDEs
Register RTL
Header files
•Implementation setup
Synthesis control file
ATPG control file
C testbench
Debugger setup
CTL, STIL gen
BSDL, IBIS gen


Thank you!